REMARKS

Claims 1-13 were pending in the application when last examined. Claims 1, 3, 12 and 13 are rejected. Claims 2 and 4-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The rejections and objections are respectfully traversed in light of the amendments above and the following remarks, and reconsideration is requested.

Response to Non-Consideration of the Information Disclosure Statement

A legible copy of each non-patent literature publication is enclosed in compliance with 37 CFR 1.98(a) (2). Applicants enclose another PTO 1449 and in light of the forgoing respectively request that the Examiner consider the art cited therein, initial, date and return to Applicants a copy thereof.

Rejections under 35 U.S.C. 103(a)

Claims 1, 3, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,870,075 A), (hereinafter referred to as Yamazaki).

The Examiner bears the initial burden of factually supporting any prima facie conclusions of obviousness. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when

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combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP §2412.

Claim 1 recites in pertinent part:

> a first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines and a relevant one of the pixel electrodes;
> a second thin film transistor connected to a previous one of the first signal lines, a previous one of the second signal lines and a relevant one of the direction control electrodes; and
> a third thin film transistor connected to the previous first signal line, the relevant second signal line and the relevant pixel electrode.

In support of the rejection, the Examiner makes reference to Fig. 1 and Fig. 2A and writes: "a third thin film transistor connected to the previous first signal line, the relevant second signal line and the relevant pixel electrode [not shown but would be the next pixel TFT connected to the pixel electrode]."

Applicants respectfully traverse the Examiner's rejection. Applicants submit that Yamazaki does not inherently disclose a thin film transistor array panel as recited in claim 1. Yamazaki discloses only two thin film transistors in a respective pixel area defined by the intersections of a first and a second signal lines. Yamazaki fails to teach or suggest "a third thin film transistor connected to the previous first signal line, the relevant second signal line and the relevant pixel electrode", as recited in claim 1. Since Yamazaki discloses only a single pixel, it follows that the next pixel area would be like the disclosed pixel area. Accordingly, "next pixel TFT" of Yamazaki, which the Examiner equates to Applicants' "third thin film transistor", would be connected to structure in the next pixel area, and would not be connected to the "relevant pixel electrode", as recited in claim 1. Instead, the said "next

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pixel TFT" in Yamazaki would be connected to the next pixel electrode in the next respective pixel area.

Applicants respectfully submit that the Examiner has failed to demonstrate how Yamazaki could be modified to provide a thin film transistor array panel according to the embodiment of Applicants' invention as in claim 1, or to prove any motivation for doing so. Therefore, the Examiner has failed to establish a prima facie case of obviousness and the Examiner's rejection of claim 1 is unsupported.

Claim 3 is amended to recite in pertinent part:

> A thin film transistor array panel comprising:
> ...
> a data wire formed on the semiconductor layer and including a plurality of data lines intersecting the gate lines, first to third source electrodes connected to the data lines, and first to third drain electrodes opposite the first to the third source electrodes with respect to the first to the third gate electrodes;
> ...
> a pixel electrode formed on the protective layer, having a plurality of cutouts, and electrically connected to the first and the third drain electrodes through the contact holes; and
> a direction control electrode connected to the second drain electrode, the direction control electrode being associated with the pixel electrode. (Emphasis added.)

In Applicants' invention according to claim 3, the array panel comprises "first to third source electrodes ... first to third drain electrodes ... first to third gate electrodes ... a pixel electrode ... electrically connected to the first and third drain electrodes ... and a direction control electrode connected to the second drain electrodes, the direction control electrode being associated with the pixel electrode." (Emphasis added). Yamazaki does not inherently disclose the thin film transistor array panel as recited in claim 3. More specifically, Yamazaki does not disclose or suggest: "first to third source electrodes connected to the data lines, and first to third drain electrodes opposite the first to third source electrodes ... a pixel electrode ... electrically connected to the first and third drain electrodes ... and a direction control

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electrode connected to the second drain electrode, the direction control electrode being associated with the pixel electrode[,]" as recited in claim 3. (Emphasis added). Yamazaki at most discloses two source electrodes, two gate electrodes and two drain electrodes in a given pixel region, which consists of one central pixel electrode and one peripheral pixel electrode surrounding the central pixel electrode (Figure 1).

Applicant respectfully submit that the Examiner has failed to demonstrate how Yamazaki could be modified to provide the thin film transistor array panel recited in claim 3 or to prove any motivation for doing so. Therefore, the Examiner has failed to establish a prima facie case of obviousness and the Examiner's rejection of claim 3 is unsupported.

Claim 12 recites in pertinent part:

> a first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines and a relevant one of the pixel electrodes;
> a second thin film transistor connected to a previous one of the first signal lines, a previous one of the second signal lines and a relevant one of the direction control electrodes;
> a third thin film transistor connected to the previous first signal line, the relevant second signal line and the relevant pixel electrode;

As described above with respect to claim 1, Yamazaki fails to teach or suggest "a third thin film transistor connected to the previous first signal line, the relevant second signal line and the relevant pixel electrode", as recited in claim 12. Accordingly, Applicants submit that the Examiner has failed to establish a prima facie case of obviousness of claim 12 and claim 13, which depends from claim 12.

Applicants respectfully request that the Examiner withdraw the rejection under 35 U.S.C § 103 of Claims 1, 3 and 12-13.

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Allowable Subject Matter

Claims 2 and 4-11 are objected to as being dependent upon a rejected base claim. The Examiner opined they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 2 depends from claim 1, and claims 4-11 depend from claim 3. For at least the reasons pointed out above, claims 1 and 3 are in condition for allowance. Applicants accordingly submit that the Examiner's objections to claims 2 and 4-11 have been rendered moot.

Accordingly, Applicants respectfully request that the Examiner withdraw the objections to claims 2 and 4-11.

CONCLUSION

In light of the above, all of the claims are in condition for allowance. Accordingly, Applicants request that a Notice of Allowance be issued. If the Examiner would care to discuss the application or has questions regarding same, please contact the undersigned at (408) 392-9250.

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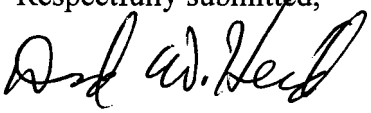
Respectfully submitted,



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